



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,082	12/06/2001	Linden Minnick	42390P12249	3183
8791	7590	10/13/2006	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			MADAMBA, GLENFORD J	
			ART UNIT	PAPER NUMBER
			2151	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/007,082	MINNICK ET AL.
	Examiner	Art Unit
	Glenford Madamba	2151

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 July 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-31 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date. _____	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION**

***Response to Remarks***

1. This action is in response to remarks filed by Applicant's representative on July 7, 2006.

***Response to Arguments***

2. Applicant's arguments filed July 7, 2006 have been fully considered but they are not persuasive.

With respect to claims 1, 11, and 20, the claims were multiply rejected under 35 U.S.C. 102(e) as being anticipated by Khanna, U.S. Patent US 6,999,995; as well as under 35 U.S.C. 102(b) as being anticipated by Johnson, U.S. Patent 5,905,874. With regards to the rejection of the claims under Khanna, and also under Johnson, Applicant argues that neither Khanna nor Johnson describes, expressly or inherently, at the least, an I/O device to "moderate one or more interrupts of an interrupt scheme on an associated computing platform if the fragment of electronic data comprises latency-sensitive data", as required by, for example, claim 1. The Office maintains that the required features are disclosed by the prior art references of Khanna and/or Johnson, and respectfully submits that Applicant has misinterpreted the prior arts of record.

Specifically, Applicant argues that embodiments of the subject application as recited in the claims disclose an I/O device that is operative to moderate interrupts based, at least in part, on one or more characteristics (e.g. latency-sensitive) of electronic data. In response to this argument, the Office maintains that both Johnson and Khanna disclose moderating interrupts according to one or more characteristics of electronic data, such as latency, as will be shown in the following discussions.

Johnson discloses as his invention a computer system for communicating with a network including a host processor, memory, an interface bus and a network interface device (e.g. NIC) for reducing data transfer latency between the computer system and the network. The network device includes a buffer for temporarily storing data, a media interface device for transferring data between the computer system's memory and the buffer, and a local processor writing a unique value at a predetermined location within the buffer, for periodically comparing the data value at the predetermined location with the unique value and for initiating data transfer from the buffer to the computer's memory when the data value does not match the unique value [Abstract].

Johnson expressly sets the context and the environment in which the moderation of the interrupts based on one or more characteristics of packets transmitted are performed. According to Applicant's own disclosure, an example of one or more of the

'characteristics' or the electronic data (packets) is *latency-sensitivity* (pg. 11, Remarks). Additionally, Applicant clearly notes that one such example of latency sensitive data or fragments of electronic data are "ACK" packets [pg.7, L20-24], and that "in the process of sending and/or receiving data packets, TCP will typically utilize an acknowledgement (ACK packet or signal) to confirm that a particular fragment or packet of electronic data was successfully delivered to a particular node on a network [pg. 6, L23-27].

Johnson discloses that "data is typically transferred across network segments in the form of packets or frames. A NIC usually includes a buffer or the like for temporarily storing data transferred between a computer system and a network".

Johnson also expressly discloses that a key parameter for determining the performance of data transmission is *data transfer latency* from the network to the computer system. Latency is a measure of the amount of time or delay to transfer a packet or packet portion to the main memory of the computer, and may further include the additional time to inform the host processor of the transfer, if necessary. In many Ethernet and token

ring schemes prior to the present invention, an entire block of data was written into the buffer for temporary storage before being transferred to the main memory. Each block formed a portion of a packet or the entire packet and is typically approximately one kilobyte in length. Transfer of each block from the NIC to the main memory depended upon whether the NIC was capable of performing direct memory access (DMA) data transfers. If so, after a block was written to the buffer of the NIC, the NIC gained control of the expansion bus of the computer and performed a

DMA transfer of the block into the computer memory. For memory-mapped configurations, the NIC informed the host processor, usually by interrupt, and the host processor controlled the transfer of the data from the buffer to the computer memory. As can be understood from the above citations, Johnson clearly discloses generating interrupts according to the transmission of packets that may lead to latency (delays). The 'packet' or 'portions of a packet' transmitted thus determine the latency of the system, and are thus 'latency-sensitive'. The Office additionally notes that claim 1 does not specifically require the type of packets to be transferred (e.g. ACK packets); only that they are sensitive to latency in general. Also, Johnson, discloses that his invention helps to "reduce latency of data transfer" [col 3, L42-45] using an 'interrupt scheme for transferring blocks of data' [col 7, L.41-55] [Fig. 5B].

Khanna similarly and expressly discloses the features recited by claim 1. Khanna discloses two types of interrupt service routines ("ISRs"). The first type of interrupts is a timer interrupt service routine. The interrupt controller\_112 periodically generates this timer ISR at periodic timer ticks of a clock signal produced by the timer logic circuit [col 4, lines 40-45]. A second type of interrupt is an "asynchronous" interrupt generated by the interrupt controller\_12 whenever the NIC 116 receives a data packet from the network 120. As emphasized by Khanna, such interrupts are asynchronous because data packets from the network 120 arrive at unexpected times depending on the network conditions such as communication traffic [col 4, lines 59-67].

Thus, Khanna clearly discloses moderating interrupts asynchronously: whenever a packet arrives and is received by NIC\_116.

Applicant also argues, however, that Khanna does not teach or disclose 'examining' the packets received as part of the interrupt routine or scheme. This is clearly not the case, as Khanna firstly discloses in one aspect of the invention that the 'data' packets sent out by computer\_100 is packaged with the assigned network address and other information in the packet header according to the given protocols [col 3, lines 36-40]. Khanna also teaches that when the "delay" (latency) between computers 100 and 130 is relatively short the computer 130 can send an acknowledgement when the delay increases, e.g., sending one ACK signal (ACK packet) to the computer 100 after every two or more data packets are received [col 6, lines 46-64]. Khanna thus discloses that 'every two or more data packets' transmitted is followed by the transmission of an ACK packet. Further, Khanna expressly discloses "processing" the data packets received (e.g. unpacketing data, performing UDP OPEN / READ / CLOSE) and examining the data to send it to the intended device for operation control, *inter alia* [col 5, lines 53-56] [col 8, lines 3-17 & 56].

Khanna therefore not only discloses the feature of generating interrupts as a result of received data that are delay / latency sensitive, in general, but also expressly discloses 'processing the received packets' and transmitting ACK signals (ACK packets) of claim 2, which is likewise disclosed and described by Applicant in the

description of the present application. The Office therefore sees no significant difference between Applicant's disclosures and those of Khanna, and the rejection of the claims are thus maintained.

As per claims 2, 4, 12, 13, 21, and 22, Applicant argues that there is no suggestion or motivation to combine the Johnson and Drottar prior art references. In response to this argument, Applicant is reminded that

Additionally, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Drottar provides, in a related endeavor and as a motivation, an improved packet format, which is more compatible with distributed computer systems in the transmission of a packets over a network [col 1, lines 65-67].

Further, it has been shown above that both Johnson and, or alternatively, Khanna disclose moderating interrupts of an interrupt scheme if the data or data

fragment comprises latency-sensitive data (e.g. ACK signals/packets). The rejection of the claims are also thus maintained at least for the same reasons provided above for Johnson and/or Khanna.

The same response is made by the Office in response to Applicant's argument with regards to the combination of Johnson and Gentry Jr.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 11, 20 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Khanna, U.S. Patent US 6,999,995.

3. As per Claims 1, 11, 20 and 29, Khanna discloses an apparatus comprising:

An input/output device (NIC\_116) [Fig. 1] being operative to:  
receive a fragment of electronic data (270) [Fig. 2] [col 5, line 57 – col 6,  
line 1];  
examine the fragment of electronic data [col 2, line 61 – col 3, line 2] [ col  
3, lines 20-45]; and  
if the fragment of electronic data comprises latency-sensitive data [col 6,  
lines 37-54], the I/O device further being operative to moderate one or  
more interrupts of an associated computing platform processor [col 1, line  
65 – col 2, line 12] [col 3, lines 3-20] [col 4, lines 40-67] [col 5, lines 16-26]  
[col 6, line 17 – col 7, line 15] [col 8, line 45 – col 9, line 2 (Claim 1)] .

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 11 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson, U.S. Patent 5,905,874.

3. Claim 1 discloses an apparatus comprising:
  - an input/output (I/O) device **210** [Figs. 2 & 3] being operative to:
    - receive a fragment of electronic data [Col 2, Lines 27-42],
    - examine the fragment of electronic data [Col 2, Lines 27-42]; and
    - if the fragment of electronic data comprises latency-sensitive data, the I/O device [Col 2, Lines 27-42] [Col 3, Lines 33-41 & Col 4, Lines 13-22] further being operative to moderate one or more interrupts of an associated computing platform processor [Col 2, Lines 48-51].

Claims 11 and 20 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

4. Claim 3 recites the apparatus of claim 1, wherein said I/O device comprises a network interface card (NIC) **210** [Col 2, lines 13-26; Col 3, lines 15-32; Figure 2 and 3].
5. Claim 5 stipulates the apparatus of claim 1, wherein said I/O device is configured to moderate by substantially immediately asserting said one or more interrupts of said associated computing platform processor [Col 2, lines 48-51 & Col 7, lines 52-56].

Claims 14 and 23 state the same limitations as Claim 2 above, and are rejected for the same reasons as they differ only by their statutory category.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2, 4, 12, 13, 21, 22, 30, 31 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Drottar et al (hereinafter Drottar), Patent Number 6,333,929.

3. Claims 2, 30 and 31 asserts the apparatus of claim 1, wherein the latency-sensitive data comprises an acknowledgement (ACK).

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), are *written in blocks of data that are in the form of packets or portions of packets (fragments)* [Col 2,

Lines 27-42]. Johnson does not disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. As can be seen in the format for data packets with a MAC header, the header format includes a field for an ACK/NAK identification and processing [Col 13, lines 1-7; also see Col 10, lines 59-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting features employed by Drottar's invention into Johnson's for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 12 and 21 state the same limitations as Claim 2 above, and are rejected for the same reasons as they differ only by their statutory category.

4. Claim 4 discloses the apparatus of claim 1, wherein the latency-sensitive data comprises one or more data packets that have a priority designation [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), are *written in blocks of data that are in the form of packets or portions of packets* (fragments) [Col 2, Lines 27-42]. Johnson does not disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. Drottar expressly teaches that the packet headers (MAC Header\_650) are comprising *a priority field*, a version field and an address field [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting feature of a field designating prioritization of packets transmitted or received, as disclosed by Drottar, into Johnson's for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 13 and 22 state the same limitations as Claim 4 above, and are rejected for the same reasons as they differ only by their statutory category.

5. Claims 6-10, 15-19, 24-28 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Gentry Jr., Patent Number 6,434,651.

6. Claim 6 points to the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts of said associated computing platform processor so that a predetermined number of interrupts per unit of time is not exceeded.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and that a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Johnson does not disclose that the network interface device is configured to moderate by deferring one or more interrupts of the host processor so that a predetermined number of interrupts per unit of time is not exceeded.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC

and transferred to a host processor are alternately enabled and disabled. In particular, after one interrupt is issued to and serviced by a host processor, another interrupt is not generated until a *predetermined period of time* has passed for a specified amount of network traffic has been sent to the host computer system. [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 1-11 & 39-67]

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the interrupt suppression features in Gentry Jr.'s invention into Johnson's so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

7. Claim 7 states the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device [Gentry Jr., Col 7, lines 19-36, 47-56, & 63-67; Col 8, lines 1-11 and 39-67].

Claims 16 and 25 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

8. Claim 8 cites the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received [Gentry Jr., Col 7, lines 47-56, & 63-67; Col 8, lines 1-11].

Claims 17 and 26 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

9. Claim 9 states the apparatus of claim 1, wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface [Gentry Jr., Col 7, lines 51-56; Col 8, lines 3-11].

Claims 18 and 27 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

10. Claim 10 identifies the apparatus of claim 1, and further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

Claims 19 and 28 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

11. Claim 15 identifies the method of claim 11, wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

12. Claim 24 states the article of claim 20, wherein said moderating comprises deferring said interrupting of said associated computing platform processor [Gentry Jr., Col 1, Lines 5-10; Figure 1; also Col 7, lines 10-18].

### ***Conclusion***

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenford Madamba whose telephone number is 571-272-7989. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarni Maung can be reached on 571-272-3932. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenford Madamba  
Examiner

Application/Control Number: 10/007,082  
Art Unit: 2151

Page 19

Art Unit 2151



JASON CARDONE  
SUPERVISORY PATENT EXAMINER